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EXAMINER	
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ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,755	KUNO, SHINJI	
	Examiner	Art Unit	
	ERNEST UNELUS	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,18-20 and 22-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,18-20 and 22-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

Applicant's arguments filed 11/11/2008 with respect to claims 1-3, 18-20, and 22-36 have been fully considered but are moot in view of the new ground(s) of rejection.

The rejection(s) of claim(s) 1-3, 18-20, and 22-35 under Shimizu et al. (US pat. 6,609,977) in view of Witt (US pub. 2004/0109005) have been fully considered and not persuasive. However, base on the amendment, a new ground(s) of rejection is made in view of Shimizu et al. (US pat. 6,609,977) and Witt (US pub. 2004/0109005).

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

INFORMATION CONCERNING DRAWINGS

Drawings

2. The applicant's drawings submitted are acceptable for examination purposes.

REJECTIONS BASED ON PRIOR ART

Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-3, 18-20, 22-25, and 28-36,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US pat. 6,609,977) in view of Witt (US pub. 2004/0109005).

5. As per **claim 1**, Shimizu discloses "An apparatus **(system 50 of fig. 2)** comprising:

a drive device **(mass storage access device 106 of fig. 2, as discloses in col. 6, line 59)**; a communication bus **(the communication bus between the main processor 110 and the graphics and audio processor 114 of fig. 2, as discloses in col. 7, lines 25-31)**;

a first processor **(Main Processor 110)** coupled to the communication bus **(see fig. 2)**, a first stream data including video data and audio data routed over the communication bus **(see col. 6, line 64 to col. 7, line 3 of Shimizu discloses, "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114. The graphics and audio processor 114 processes these commands to generate interesting visual images on display 59 and interesting stereo sound on stereo loudspeakers 61R, 61L or other suitable sound-generating devices". The main processor generating these commands is a form of decoding. Obviously, the processor gets the data to generate. Also, the claim language is not specific as to how the 'decoding' happens)**;

a second processor **(Graphics and Audio Processor 114)** provided with a second stream data including video data and audio data **('audio output of mass storage access device 106')** received from the drive device without being routed over the communication bus **(col. 7, lines 13-17, discloses "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device 106. See col. 6, lines 56-59, which discloses "Main processor 110 interactively responds to user inputs, and executes a video game or other program supplied for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive"; in other words, the mass storage device 106 is also there to receive video data)". In other word, the graphics and audio processor receives from the mass storage access device and transmits to the audio codec)**, the second processor to decode the second stream data to reproduce the second stream data in accordance with an instruction sent from the first processor over the communication bus **(in regards to this limitation, fig. 2, shows the audio codec to decode the 'audio output of mass storage access device 106'. Also, col. 6, lines 64-66, discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". In other word, as the 'main' processor generates instructions to be executed by the graphics and audio processor, such as how the graphics and audio processor processes I/O. Also, as disclose in col. 8, lines 21-23, "Main processor 110 communicates streams of data (e.g., graphics command streams and display lists) to command processor 200"; note, this command**

processor is inside the graphics and audio processor. See also col. 6, lines 56-59 for further detail),

but fails to specifically disclose the first processor to receive and decode a first stream of data.

Witt discloses a processor **(IOP 700 of fig. 6)** to receive and decode a first stream of data **(see paragraph 0067, which discloses, "At the output stage the hardware module 904 may be used to convert output video and audio into DV format which is output via the iLink port 702").**

Shimizu et al. (US pat. 6,609,977) and Witt (US pub. 2004/0109005) are analogous art because they are from the same field of endeavor of video data processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a serial interface for interfacing an audio and graphics coprocessor with a variety of different types of accessory devices including but not limited to hand-held game controllers as taught by Shimizu and a video processing method for preparing an anti-aliased foreground image for display over an image background as taught by Witt.

The motivation for doing so would have been because Witt teaches, "The IOP 700 has a Direct Memory Access (DMA) architecture to facilitate rapid data transfer rates" (**see paragraph 0035**).

Therefore, it would have been obvious to combine Witt (US pub. 2004/0109005) and Shimizu et al. (US pat. 6,609,977) for the benefit of creating the apparatus to obtain the invention as specified in claim 1.

6. As per **claim 2**, combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Shimizu further discloses "wherein the second processor is a stream processor" **(col. 7, lines 13-17 discloses the graphics and audio processor to be processing audio stream, as also discloses in fig. 2).**

7. As per **claim 3**, combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Shimizu further discloses wherein the first processor is a central processing unit (CPU) **(see col. 6, line 50)**.

8. As per **claim 18**, combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Shimizu further discloses wherein the drive device is a hard disk drive **(see hard disk drive 62 of fig. 2).**

9. As per **claim 19**, Shimizu discloses "An apparatus **(system 50 of fig. 2)** comprising:

a drive device **(mass storage access device 106 of fig. 2, as discloses in col. 6, line 59)**; a communication bus **(the communication bus between the main processor 110 and the graphics and audio processor 114 of fig. 2, as discloses in col. 7, lines 25-31)**;

a first processor **(Main Processor 110)** coupled to the communication bus **(see fig. 2)**, a first stream data including video data and audio data routed over the communication bus **(see col. 6, line 64 to col. 7, line 3 of Shimizu discloses, "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114. The graphics and audio processor 114 processes these commands to**

generate interesting visual images on display 59 and interesting stereo sound on stereo loudspeakers 61R, 61L or other suitable sound-generating devices". The main processor generating these commands is a form of decoding. Obviously, the processor gets the data to generate. Also, the claim language is not specific as to how the 'decoding' happens);

a second processor **(Graphics and Audio Processor 114)** provided with a second stream data including video data and audio data **('audio output of mass storage access device 106')** received from the drive device without being routed over the communication bus **(col. 7, lines 13-17, discloses "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device 106. See col. 6, lines 56-59, which discloses "Main processor 110 interactively responds to user inputs, and executes a video game or other program supplied for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive"; in other words, the mass storage device 106 is also there to receive video data)". In other word, the graphics and audio processor receives from the mass storage access device and transmits to the audio codec)**, the second processor to decode the second stream data to reproduce the second stream data in accordance with an instruction sent from the first processor over the communication bus **(in regards to this limitation, fig. 2, shows the audio codec to decode the 'audio output of mass storage access device 106'. Also, col. 6, lines 64-66, discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". In other word, as the 'main' processor generates instructions to be executed by the graphics and audio**

processor, such as how the graphics and audio processor processes I/O. Also, as disclose in col. 8, lines 21-23, "Main processor 110 communicates streams of data (e.g., graphics command streams and display lists) to command processor 200"; note, this command processor is inside the graphics and audio processor. See also col. 6, lines 56-59 for further detail), and a network control unit **(controllers 52, as discloses in fig. 1)** coupled **(col. 6, lines 25 –27, discloses that it can be coupled wirelessly or through a cables)** to the communication bus **(see fig. 1)**, the network control unit to transmit the first stream data via the communication bus **(see col. 6, lines 53-55, which discloses "In this example, main processor 110 (e.g., an enhanced IBM Power PC 750) receives inputs from handheld controllers 52", the controller is indirectly causing the main processor to transmit a command, using the communication bus, to audio processor 114)**.

but fails to specifically disclose the first processor to receive and decode a first stream of data.

Witt discloses a processor **(IOP 700 of fig. 6)** to receive and decode a first stream of data **(see paragraph 0067, which discloses, "At the output stage the hardware module 904 may be used to convert output video and audio into DV format which is output via the iLink port 702").**

Shimizu et al. (US pat. 6,609,977) and Witt (US pub. 2004/0109005) are analogous art because they are from the same field of endeavor of video data processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a serial interface for interfacing an audio and graphics coprocessor with a variety of different types of accessory devices including but not limited to hand-held game

controllers as taught by Shimizu and a video processing method for preparing an anti-aliased foreground image for display over an image background as taught by Witt.

The motivation for doing so would have been because Witt teaches, "The IOP 700 has a Direct Memory Access (DMA) architecture to facilitate rapid data transfer rates" (**see paragraph 0035**).

Therefore, it would have been obvious to combine Witt (US pub. 2004/0109005) and Shimizu et al. (US pat. 6,609,977) for the benefit of creating the apparatus to obtain the invention as specified in claim 19.

10. As per **claims 20 and 34,** combination of Shimizu and Witt discloses "The apparatus according to claim 19," **[See rejection to claim 19 above]**, Witt further discloses wherein the control unit includes an IEEE 1394 processor".**(see paragraph 0035, which discloses the IOP 700, as a control unit being an IEEE 1394 processor).**

11. As per **claim 22**, the combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Witt further discloses, "wherein the communication bus is a Peripheral Component Internet (PC1) bus" **(see paragraph 0065).**

12. As per **claim 23**, the combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Shimizu further discloses: a video bus **(the communication bus between the main processor video/encoder 120 and the graphics and audio processor 114, as discloses in fig. 2)**; and a graphic controller **(Graphics and Audio**

Processor 114), which has a 3D Graphics processor) in communication with the first processor and the second processor **(see fig. 3)**, the graphic controller to convert the decoded first stream data into display video signals and to transmit the display video signals to the second processor over the video bus **(see fig. 3)**.

13. As per **claims 24 and 29**, the combination of Shimizu and Witt discloses "The apparatus according to claim 23," **[See rejection to claim 23 above]**, Shimizu further discloses wherein the second processor superposes the display video signals transmitted over the video bus on a video image generated from the decoded second stream data in accordance with display information transferred from the first processor to the second processor over the communication bus **(see fig. 2 and col. 7, lines 13-17, which discloses "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device 106)". In other word, the graphics and audio processor receives from the mass storage access device and transmits to the audio codec. Also, col. 6, lines 64-66, discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". In other word, as the 'main' processor, it generate instructions to be executed by the graphics and audio processor, such as how the graphics and audio processor to process I/O. as also discloses in col. 8, lines 21-23, "Main processor 110 communicates streams of data (e.g., graphics command streams and display lists) to**

command processor 200"; note, this command processor is inside the graphics and audio processor).

14. As per **claims 25 and 30**, the combination of Shimizu and Witt discloses "The apparatus according to claim 24," **[See rejection to claim 24 above]**, Shimizu further discloses wherein the display information includes information designating a region in a drawing area and a transparency rate at the display video signals on a screen **(see col. 57 line 36 to col. 58, line 8)**.

15. As per **claim 28**, Shimizu discloses "An apparatus **(system 50 of fig. 2)** comprising:

a communication bus **(the communication bus between the main processor 110 and the graphics and audio processor 114, as discloses in col. 7, lines 25-31)**;

a drive device **(mass storage access device 106 of fig. 2, as discloses in col. 6, line 59)**; a video terminal **(video encoder 120 of fig. 2)**;

a first processor **(Main Processor 110)** coupled to the communication bus **(see fig. 2)**, a first stream data including video data and audio data sent over the communication bus **(see col. 6, line 64 to col. 7, line 3 of Shimizu discloses, "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114. The graphics and audio processor 114 processes these commands to generate interesting visual images on display 59 and interesting stereo sound on stereo loudspeakers 61R, 61L or other suitable sound-generating devices". The main processor generating these commands is a form of decoding. Obviously, the processor gets the data to generate. Also, the claim language is not specific as to how the 'decoding' happens)**; and

a second processor **(Graphics and Audio Processor 114)** coupled to the drive device, the video terminal, and the first processor **(see fig. 2)**, the second processor being provided with a second stream data including video data and audio data **('audio output of mass storage access device 106')** that is sent from the drive device without use the communication bus **(col. 7, lines 13-17, discloses "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device 106. See col. 6, lines 56-59, which discloses "Main processor 110 interactively responds to user inputs, and executes a video game or other program supplied for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive"; in other words, the mass storage device 106 is also there to receive video data)". In other word, the graphics and audio processor receives from the mass storage access device and transmits to the audio codec)**, the second processor to (i) decode the second stream data for reproducing the second stream data in accordance with an instruction sent from the first processor via the communication bus and (ii) display video signals, that are based on the decoded first stream data and transmitted by the first processor over a video bus separate from the communication bus, on the video terminal **(in regards to this limitation, fig. 2, shows the audio codec to decode the 'audio output of mass storage access device 106'. Also, col. 6, lines 64-66, discloses "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114". In other word, as the 'main' processor generates instructions to be executed by the graphics and audio processor, such as how the graphics and audio processor processes I/O. Also, as disclose in**

col. 8, lines 21-23, "Main processor 110 communicates streams of data (e.g., graphics command streams and display lists) to command processor 200"; note, this command processor is inside the graphics and audio processor. See also col. 6, lines 56-59 for further detail).

but fails to specifically disclose the first processor to receive and decode a first stream of data.

Witt discloses a processor **(IOP 700 of fig. 6)** to receive and decode a first stream of data **(see paragraph 0067, which discloses, "At the output stage the hardware module 904 may be used to convert output video and audio into DV format which is output via the iLink port 702").**

Shimizu et al. (US pat. 6,609,977) and Witt (US pub. 2004/0109005) are analogous art because they are from the same field of endeavor of video data processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a serial interface for interfacing an audio and graphics coprocessor with a variety of different types of accessory devices including but not limited to hand-held game controllers as taught by Shimizu and a video processing method for preparing an anti-aliased foreground image for display over an image background as taught by Witt.

The motivation for doing so would have been because Witt teaches, "The IOP 700 has a Direct Memory Access (DMA) architecture to facilitate rapid data transfer rates" (**see paragraph 0035**).

Therefore, it would have been obvious to combine Witt (US pub. 2004/0109005) and Shimizu et al. (US pat. 6,609,977) for the benefit of creating the apparatus to obtain the invention as specified in claim 28.

16. As per **claim 31** the combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Shimizu further discloses wherein the first stream data is received from a first source and the second stream of data is received from a second source different than the first source **(see col. 6, line 64 to col. 7, line 3 of Shimizu discloses, "In this example, main processor 110 generates 3D graphics and audio commands and sends them to graphics and audio processor 114. The graphics and audio processor 114 processes these commands to generate interesting visual images on display 59 and interesting stereo sound on stereo loudspeakers 61R, 61L or other suitable sound-generating devices". See also col. 7, lines 13-17, which discloses, "Audio codec 122 can receive audio inputs via a buffer 124 and provide them to graphics and audio processor 114 for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device 106. See col. 6, lines 56-59, which discloses "Main processor 110 interactively responds to user inputs, and executes a video game or other program supplied for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive"; in other words, the mass storage device 106 is also there to receive video data)". In other word, the graphics and audio processor receives from the mass storage access device and transmits to the audio codec)**.

17. As per **claim 32** the combination of Shimizu and Witt discloses "The apparatus according to claim 31," **[See rejection to claim 31 above]**, Shimizu further discloses wherein the first stream data is received via a connector **(Main Processor 110)** being different than the second source being a drive device **(see fig. 2)**.

18. As per **claim 33** the combination of Shimizu and Witt discloses "The apparatus according to claim 28," **[See rejection to claim 28 above]**, Shimizu further discloses wherein the first stream data is received from a source different than the drive device **(see fig. 2)**.

19. As per **claim 35**, the combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Witt further discloses, "wherein the first stream data is in an encoded format when routed over the communication bus prior to the first processor decoding the first data stream **(see paragraph 0069).**

20. **Claims 26 and 27,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US pat. 6,609,977) in view of Witt (US pub. 2004/0109005), as applied to claim 1, and further in view of Ochiai et al. (US pat. 6,757,482).

21. As per **claim 26,** the combination of Shimizu and Witt discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, including a third stream data to the second processor for storage into a storage medium associated with the drive device **(see fig. 2**

and col. 7, lines 25-31 of Shimizu), but fails to specifically disclose a television tuner adapted to transmit a third stream data to the second processor for storage into a storage medium associated with the drive device.

Ochiai discloses wherein a television tuner adapted to transmit a third stream data to the second processor for storage into a storage medium associated with the drive device **(see col. 5, lines 23-30 and fig. 2).**

Shimizu et al. (US pat. 6,609,977), Witt (US pub. 2004/0109005), and Ochiai et al. (US pat. 6,757,482) are analogous art because they are from the same field of endeavor of video data processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a serial interface for interfacing an audio and graphics coprocessor with a variety of different types of accessory devices including but not limited to hand-held game controllers as taught by Shimizu, a video processing method for preparing an anti-aliased foreground image for display over an image background as taught by Witt, and a method and a device for dynamically editing broadcast data (terrestrial or satellite) or cablecast data received by a receiving terminal (TV tuner etc.) as taught by Ochiai.

The motivation for doing so would have been because Ochiai teaches a TV tuner allow you to receive broadcast data (video data and audio data) of broadcast programs **(col. 5, lines 23-30).**

Therefore, it would have been obvious to combine Ochiai et al. (US pat. 6,757,482), Witt (US pub. 2004/0109005), and Shimizu et al. (US pat. 6,609,977) for the benefit of creating the apparatus to obtain the invention as specified in claim 26.

22. As per **claim 27**, the combination of Shimizu, Witt, and Ochiai discloses "The apparatus according to claim 1," **[See rejection to claim 1 above]**, Ochiai discloses a television tuner **(see fig. 2)** and Shimizu further discloses "a transport stream bus **(parallel bus 130 of fig. 2)** coupled to the second processor, the transport stream bus enables transmission of the third stream data to the second processor without using the communication bus" **(see col. 7, lines 25-31).**

23. As per **claim 36**, the combination of Shimizu, Witt, and Ochiai discloses "The apparatus according to claim 28," **[See rejection to claim 28 above]**, Witt discloses wherein the first stream data is in an encoded format when routed over the communication bus prior to the first processor decoding the first stream data **(see paragraph 0065)**.

RELEVANT ART CITED BY THE EXAMINER

24. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

25. The following reference teaches an apparatus comprising; a communication bus; a drive device; a video terminal; a first and a second processor.

U.S. PATENT NUMBER

US 2004/0208492 and 2004/0018000

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

26. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

27. Per the instant office action, claims 1-3, 18-20, and 22-36 have received a final action on the merits.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

29. If attempts to reach the above noted Examiner by telephone is unsuccessful, the Examiner's supervisor, Mr. Alford Kindred , can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 12, 2009

Ernest Unelus
Examiner
Art Unit 2181

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

/E. U./
Examiner, Art Unit 2181